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(54) Wafer sensing and clamping monitor.

(57) A wafer position and clamp sensor. A circuit 114 monitors capacitance between two electrodes 22,24 within a wafer support 14,16,18,20. With no wafer 12 on the support, the capacitance falls in one range, with the wafer in place but not clamped, the capacitance falls in a second range and with the wafer held in place by an electrostatic attraction the capacitance falls in a third range. The sensed capacitance is converted to a frequency and then a DC voltage level 164 that can easily be sensed and used to confirm wafer placement and then confirm wafer clamping.

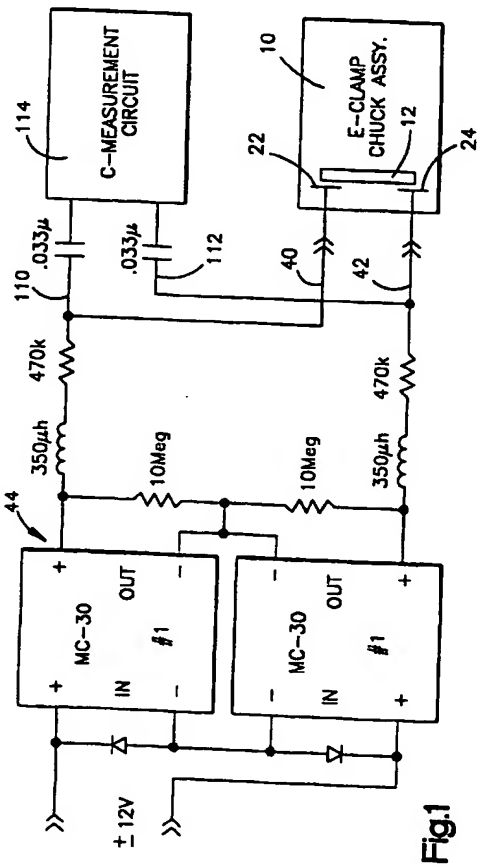

Fig.1

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Field of the Invention

The present invention concerns method and apparatus for holding a semiconductor wafer against a wafer support and more particularly to method and apparatus for monitoring operation of such apparatus.

Background Art

U.S. Patent No. 5,103,367, entitled *Electrostatic Chuck Using AC Field Excitation* relates to a mechanism for holding semiconductor wafers in contact with a support during treatment of the wafers. The '367 patent discloses three electrodes, two of which define a substantially planar surface and are embedded within a thin dielectric film. These two electrodes are excited by a low-frequency AC supply to produce sine wave fields of controlled amplitude and phase. The third electrode provides a reference point for the other two electrodes. By controlled rates of voltage application and removal, low-voltage gradients are obtained on the wafer support. This results in no retentive forces between the dielectric medium and the wafer. A low alternating current amplitude excitation of the chuck enables capacitative current sensing of the relative positions of the wafers and the dielectric film enabling simple control of voltage application to the electrodes.

Disclosure of the Invention

The present invention concerns a method and apparatus for securing a silicon wafer to a wafer support. The presence of the silicon wafer on the support is sensed by measuring the capacitance between two electrodes attached to the support. Once the measured capacitance between the two electrodes reaches a value indicating a wafer has been placed on the support, the wafer is secured to the support by creating an electrostatic attraction between the wafer and the support. A change in capacitance between the two electrodes as the electrostatic attraction is created is used as a check to make sure the wafer has been secured to the support by the electrostatic attraction.

Apparatus constructed in accordance with one embodiment of the invention secures a silicon wafer to a wafer support and includes a wafer support including two electrodes for attracting wafers to the wafer support by means of an electrostatic attraction. Capacitance monitoring circuitry coupled to the electrodes monitors a capacitance between the two electrodes. A power supply energizes the two electrodes. A controller applies energization signals from the power supply to the two electrodes, thereby attracting the wafer to the wafer support once a wafer has been placed into the wafer support. The controller includes an input coupled to an output from the capacitance monitoring circuitry to determine a presence of the wafer on the wafer support.

More particularly, an electrostatic chuck for semiconductor wafers constructed in accordance with a preferred embodiment of the invention includes a first dielectric layer engageable by a wafer; a base member supporting said first dielectric layer; first and second electrodes positioned between said first dielectric layer and said base member; and a power supply to apply a DC electric potential to the first and second electrodes to create an electrostatic attractive force between the first dielectric layer and said wafer. Capacitance sensing circuitry senses capacitance between the first and second electrodes and monitors a change in said capacitance as the wafer is placed on the first dielectric layer. The capacitance sensing circuitry also monitors a change in said capacitance as the wafer is held in place by the electrostatic attractive force.

The above and other objects, advantages and features of the invention will become better understood from detailed description of a preferred embodiment of the invention which is described in conjunction with the accompanying drawings.

Brief Description of the Drawings

Figure 1 is a schematic showing a power supply, electrostatic clamp assembly and capacitance measuring circuit;
Figure 2 is a plan view of a wafer support used in an ion implanter;
Figure 3 is a view as seen from the plane 3-3 in Figure 2;
Figures 4 and 4A are schematics of a capacitance sensing circuit;
Figure 5 is a power supply circuit for energizing the sensing circuit of Figures 4 and 4A; and
Figure 6 is a schematic of a control system that utilizes an output of the capacitance sensing circuit of Figures 4 and 4A to control an ion implanter.

Best Mode For Practicing the Invention

The drawings illustrate a clamp assembly 10 for supporting and holding a semiconductor wafer 12 (Fig. 3) for processing. The clamp assembly 10 includes a backing plate 14 which is preferably formed of alumina or molybdenum, a base member 16 also formed of alumina, a dielectric layer 18 of glass, and a dielectric layer 20 of alumina. Electrodes 22, 24 are interposed between the glass layer 18 and the dielectric layer 20 and a heating element 26 is interposed between the glass layer and the base member 16.

A gas fitting 28 extends through the chuck assembly opening into the interface between the wafer

and the layer 20 to provide gas conduction cooling between the wafer and the chuck as described in U.S. Patent No. 4,261,762. A gas distribution groove 29 is formed in the top surface of layer 20 to aid in the distribution of the gas.

The base member 16 defines a manifold having a channel 30 for the flow of a cooling fluid. In the preferred embodiment shown, the channel is formed as a spiral; however, it can also follow a meandering path or it can be a series of interconnected channels. The channels are closed to define an enclosed conduit or conduits by means of the backing plate 14, which is sealed against the manifold. Openings are provided in the backing plate for a coolant inlet fitting 32 and a coolant outlet fitting 34. Since the present chuck assembly is intended to perform under a wide range of temperature conditions, the cooling medium flowing through the manifold can be either a liquid or a gas, depending on the application.

Clamp Construction

The dielectric layer 20 is preferably formed of a thin (about .25 mm) layer of high purity (99.5%) alumina. The electrodes 22 and 24 are then formed on the bottom (as seen in Fig. 2) surface of the dielectric layer, preferably by screen printing a paste of powdered copper aluminum or silver palladium metals and glass frit onto the dielectric layer and then firing it at about 700°C. As shown in Figure 1, the electrodes are essentially half circular in plan view.

The heating element 26 is formed by screen printing a paste of powdered tungsten and glass frit onto the manifold in the form of a continuous meander, the geometry of the meander preferably being as shown in Figure 3 to provide a higher heater power density at the outer edge to optimize temperature uniformity across the chuck.

Once the electrodes 22, 24 and heating element 26 are fired onto the dielectric layer, the layer 20 is bonded to the manifold. After the above assembly is complete, the backing plate 14 is furnace brazed or sealed by means of a sealing glass to the bottom of the manifold 16.

As shown schematically in Figure 3, access holes 36, 38 are formed through the backing plate 14, the manifold 16 and the dielectric layer 18 for a first conductor 40 connected to the electrode 22 and for a second conductor 42 connected to the electrode 24. The conductors 40, 42 are attached to the electrodes by brazing or other convenient methods such as by providing spring contacts engageable with the electrodes and are connected to a switching power supply 44 (Fig. 1) which provides a signal of about 3 kilovolts DC to create the electrostatic clamping force to a semiconductor wafer 12 placed on the surface of the dielectric layer 20.

Access holes 46, 48 are also formed through the backing plate 14 and the manifold 16 for a third conductor 50 attached to one terminal of heating element 26 also by brazing or the like, and fourth conductor 52 similarly attached to the other terminal of heating element 26 to connect the heating element to a second power source 54, typically operating at 120 volts. Preferably, the access holes 36, 38 and the hole for the gas fitting 28 are machined into the structure with the holes 36, 38 sealed with sealing glass and the fitting bonded into its hole with sealing glass.

Capacitance Sensing Circuit

As seen in Figure 1, two inputs 110, 112 from the electrodes 22, 24 are coupled to a capacitive sense circuit 114. A capacitance across these two inputs 110, 112 corresponds to the capacitance between the electrodes 22, 24 and is influenced by the presence of a wafer as well as the voltage applied to the electrodes. These two inputs are coupled to an operational amplifier 120 within an integrated circuit 122. The integrated circuit is a commercially available circuit designated LF 356 and can be obtained from National Semiconductor.

The operational amplifier 120 generates an output which oscillates with a frequency directly related to the capacitance between the inputs 110, 112.

The oscillating output signal from the operational amplifier 120 varies between plus and minus 9 volts. This signal is rectified and shaped and then coupled to a comparator amplifier 130 having a reference input 132 defined by a zener diode 134 at 3 volts. The comparator amplifier 130 creates a square wave signal output having a fixed 10 microsecond ON period whose frequency varies depending on the sensed capacitance. For a 4-inch circular diameter wafer, this period is approximately 20 microseconds with no wafer in place, 30 microseconds with a wafer placed on the layer 20, and 40 microseconds with the wafer in place and a clamping voltage (approximately 3 kilovolts) applied to the electrodes by the power supply 44.

An output from the comparator amplifier 130 turns on and off light-emitting diodes 140, 142 which are optoisolated from corresponding photodetectors. A top photodetector 144 is used for diagnostic purposes and an output 148 from the detector 144 can be coupled to an oscilloscope, for example, for monitoring frequency changes with capacitance.

A second photodetector 146 generates a signal which turns on and off a transistor 150 which is coupled to an analog switch 152 (Fig. 4A). This analog switch 152 has in input (IN) coupled to the collector of the transistor 150. As the transistor turns on and off, outputs (S1, S2) of the switch 152 sequentially change state from ground to 8 volts in accordance with the square wave frequency output from the comparator 130.

The output from the analog switch 152 is integrated by a resistor, capacitor circuit 154 so that the input to a non-inverting input 160 of an operational amplifier 162 is a voltage level directly related to the capacitance sensed by the circuit 114. This operational amplifier 162 operates as a voltage follower so that an output 164 designated FVOUT is a DC output signal directly related to sensed capacitance. This DC output signal is used by an implanter control system 250 (Fig. 6) to monitor performance of the system. The wafer handler for depositing a wafer onto the chuck is activated in response to an appropriate no wafer condition being sensed. Once the wafer is sensed, an output from the control circuit 250 activates the DC power supply 44 to energize the electrodes 22, 24 causing an electrostatic attraction between the clamp and the wafer.

Turning to Figure 5, this figure discloses a power supply circuit 200 for generating voltages appropriate for the capacitance monitoring circuit 114. Two inputs 210, 212 at the left of Figure 5 provide a 12 volt signal which energizes a light-emitting diode 213. The 12-volt signal is then coupled to integrated circuit voltage regulators 216, 218 for producing +8 and +5 volts. A DC to DC converter 220 provides plus and minus 15-volt signals. These voltages are applied to the circuitry of Figures 4, 4A for providing the capacitance monitoring capability of the present invention.

Operation

In operation, a wafer 12, which is to be held within an ion beam for processing, is placed upon the surface of the layer 20, and the supply 44 will be energized to apply an electrostatic attractive force between the wafer and the layer 20 sufficient to maintain the wafer in position on the chuck. The chuck 10 can then be both rotated and translated to bring the wafer into the ion implantation path of the ion beam.

The implanter control system 250 (Fig. 6) has a large number of device interfaces which receive inputs from sensors 252 (for example, gauges measuring pressures, voltmeters, encoders measuring mechanical position, and the FVOUT output 164), and send operating commands to mechanical and electrical components 254 (for example, valves, power supplies, robots, and the electrostatic clamp power supply 44).

Within the control system there are programmed a variety of cross checks which must be performed before sending an operating command (for example, the valve to a cryopump cannot be opened unless it is verified that the chamber is already under rough vacuum). The output 164 indicates the wafer's presence and whether it is clamped and provides critical information for these cross checks to implement wafer handling and implantation operations. For example, the assembly 10 would not be rotated into a vertical position unless the wafer was verified to be securely clamped. Similarly, the clamp would not be activated unless the wafer's presence on the clamp was verified. When a critical cross check fails, the control system 250 has the ability to place the implanter into HOLD (suspend further operation) in order to avoid damage to the machine or to produce wafers.

A second function of the series of cross checks is to provide an operator interface 260 information about machine status. Specifically, when a cross check fails, an alarm message is generated for display on an operator interface screen, and is recorded in a data log maintained on a disk drive. This information permits an operator to take corrective action to restore normal machine operation.

Figure 6 represents current state-of-the-art for equipment of this type, and the addition of the capacitive sensing circuit 114 represents an advance in the quality of information available about the status of the wafer on the clamp 10.

While the preferred embodiment of the invention has been described with a degree of particularity, it is the intent that the invention include all modifications and alterations from the disclosed design falling within the spirit or scope of the appended claims.

Claims

1. A method for securing a semiconductor wafer 12 to a wafer support 14,16,18,20 characterized by the steps of:
   a) sensing the presence of the semiconductor wafer 12 on the wafer support 14,16,18,20 by measuring the capacitance between two electrodes 22,24 attached to the support;
   b) once the measured capacitance between the two electrodes 22,24 reaches a value indicating a wafer 12 has been placed on the support 14,16,18,20 securing the wafer to the support by creating an electrostatic attraction between the wafer and the support; and
   c) monitoring a change in capacitance between the two electrodes 22,24 as the electrostatic attraction is created to assure the wafer 12 has been secured to the support by the electrostatic attraction.

2. The method of Claim 1 wherein the step of securing the wafer is characterized by applying a direct current voltage 44 between the two electrodes 22,24.

3. The method of Claim 1 wherein the monitoring step is characterized by a substep of generating a warning message and suspending movement of the wafer support to an implant position if proper clamping of the wafer is not sensed.

4. Apparatus for securing a semiconductor wafer 12 to a wafer support 14,16,18,20 that includes two electrodes 22,24 for attracting wafers to the wafer support by means of an electrostatic attraction characterized by:

b) capacitive sensing circuitry 114 coupled to the electrodes 22,24 for monitoring a capacitance between the two electrodes;

c) a power supply 44 for energizing the two electrodes 22,24; and

d) a controller 250 to apply energization signals from the power supply to the two electrodes, thereby attracting the wafer to the wafer support once a wafer has been placed into the wafer support;

e) said controller including an input coupled to an output from the capacitive sensing circuitry corresponding to a sensed capacitance indicating a presence of the wafer on the wafer support.

5. The apparatus of Claim 4 wherein the controller 250 is characterized by means for monitoring an attraction produced by the power supply based upon sensed capacitance between the electrodes once a power supply voltage has been applied to the electrodes.

6. The apparatus of Claim 6 further charactereized by robotic means 254 coupled to the controller 250 for re-orienting the wafer support and moving said wafer into an ion implant orientation, said controller including means for de-activating the robotic means if the controller senses inadequate electrostatic attraction between the wafer and the wafer support based upon sensed capacitance.

7. The apparatus of claim 4 wherein the controller 250 is characterized by means for monitoring a change in said capacitance as the wafer is brought into contact with the first dielectric layer and for further monitoring a change in said capacitance as the wafer is held against the first dielectric layer by the electrostatic attraction.

8. The apparatus of Claim 7 wherein the capactive sensing circuitry 114 is characterized by an oscillator circuit 120 having a frequency that changes as the capacitance between said first and second electrodes changes.

9. The apparatus of Claim 8 wherein the means for sensing further is characterized by an integrator circuit 154 coupled to the oscillator circuit for converting the frequency signal to a voltage level.

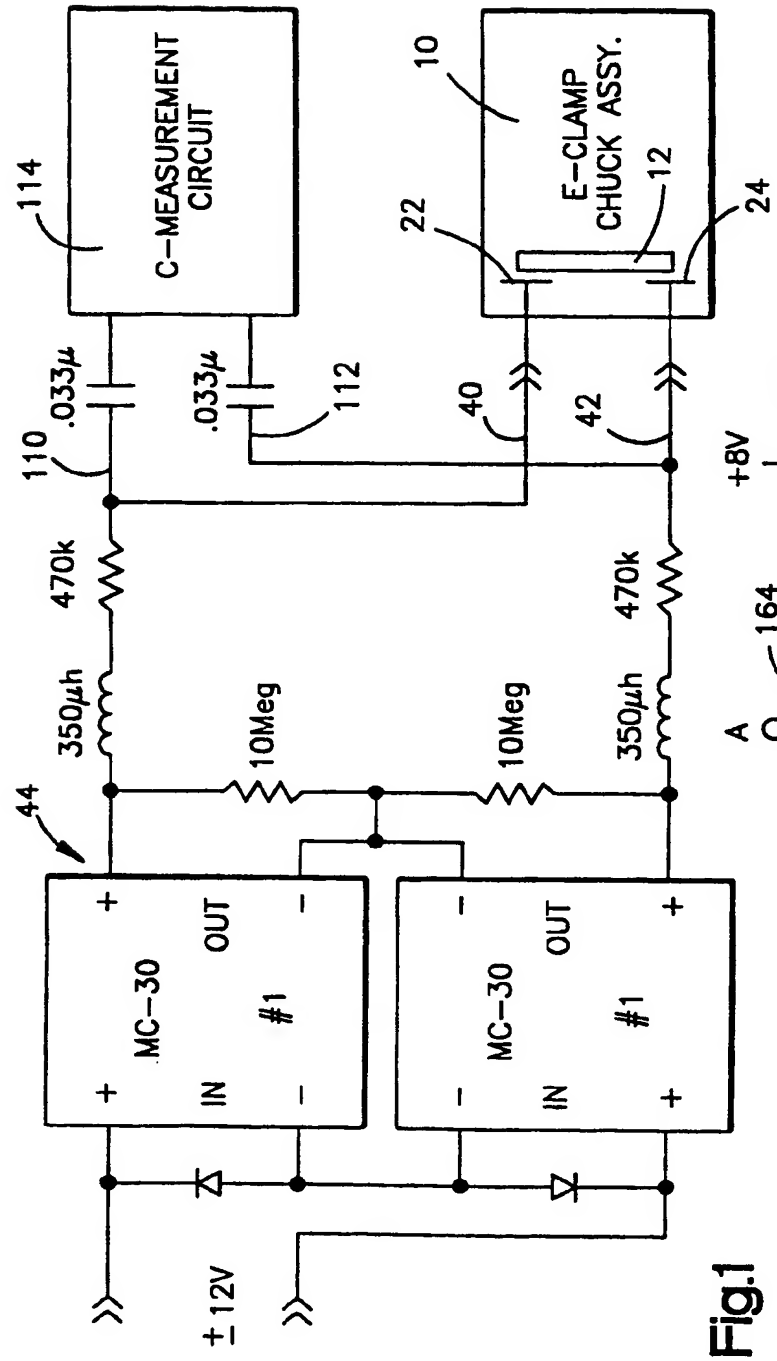

Fig.1

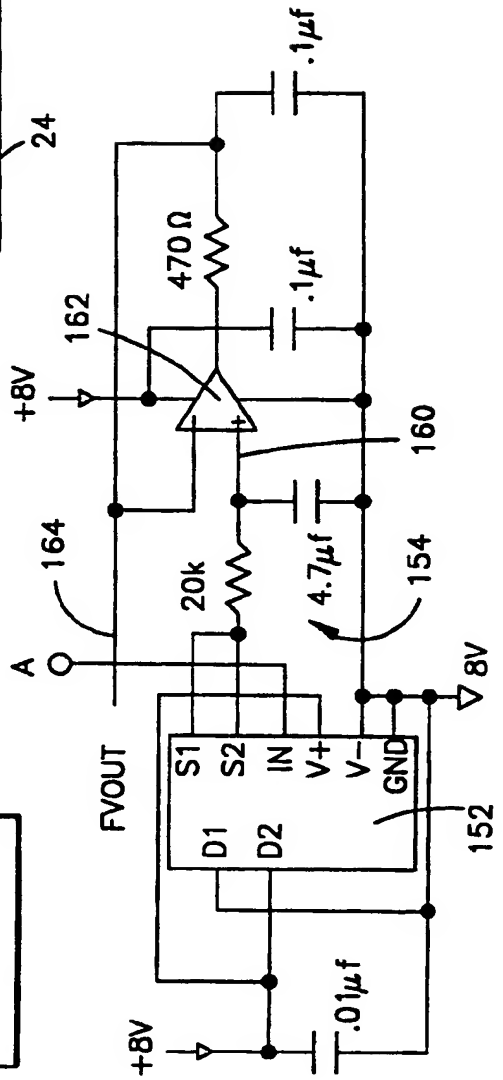

Fig.4A

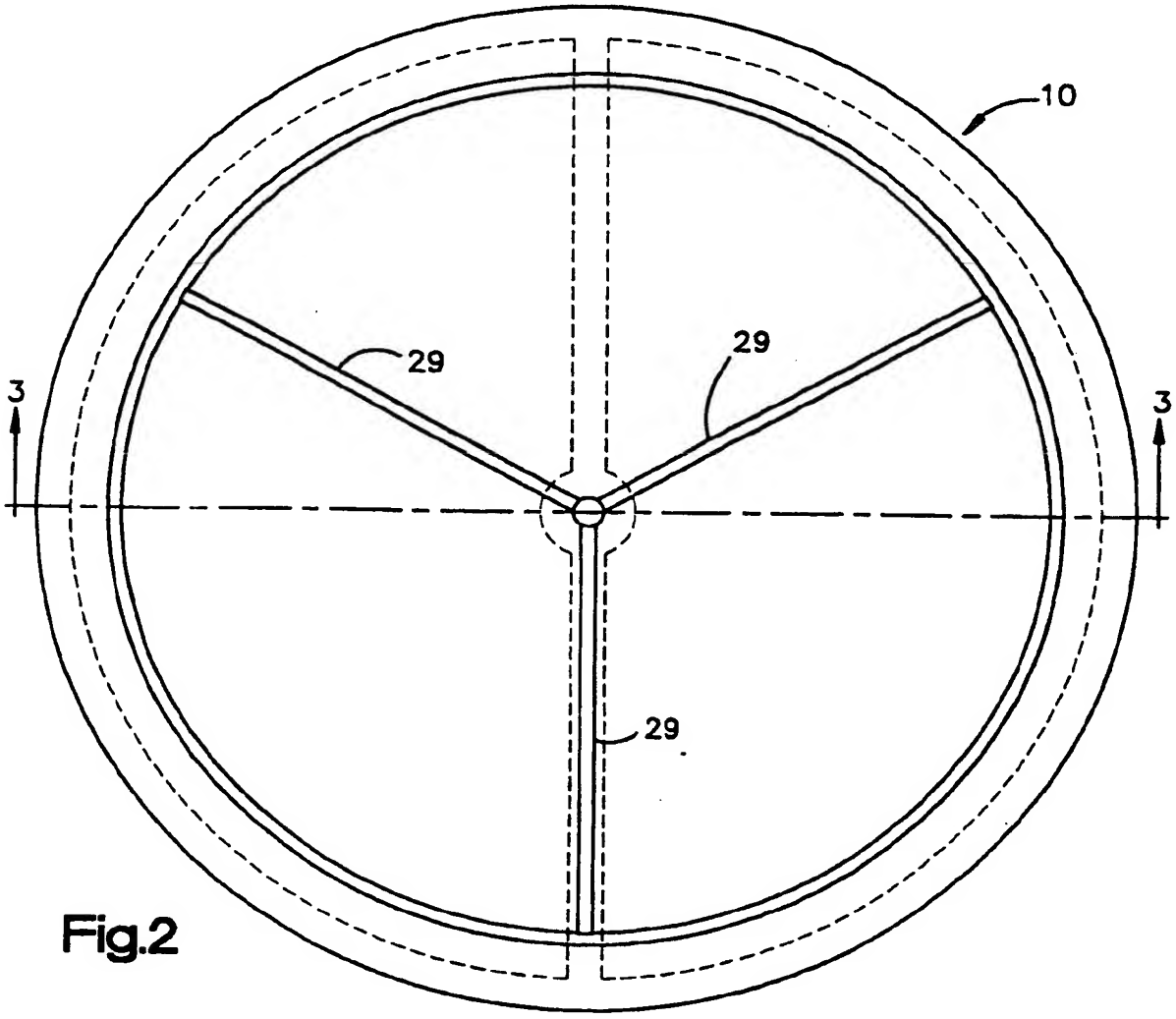

Fig.2

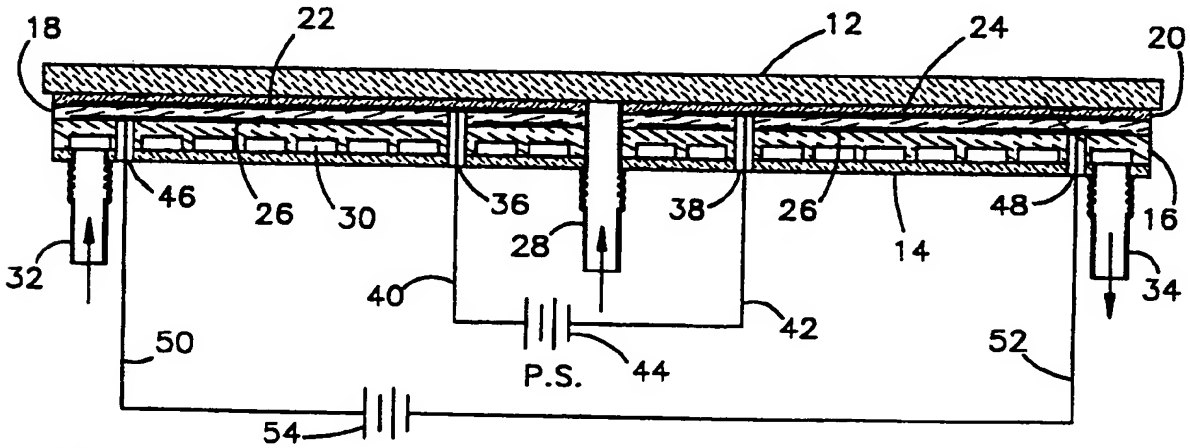

Fig.3

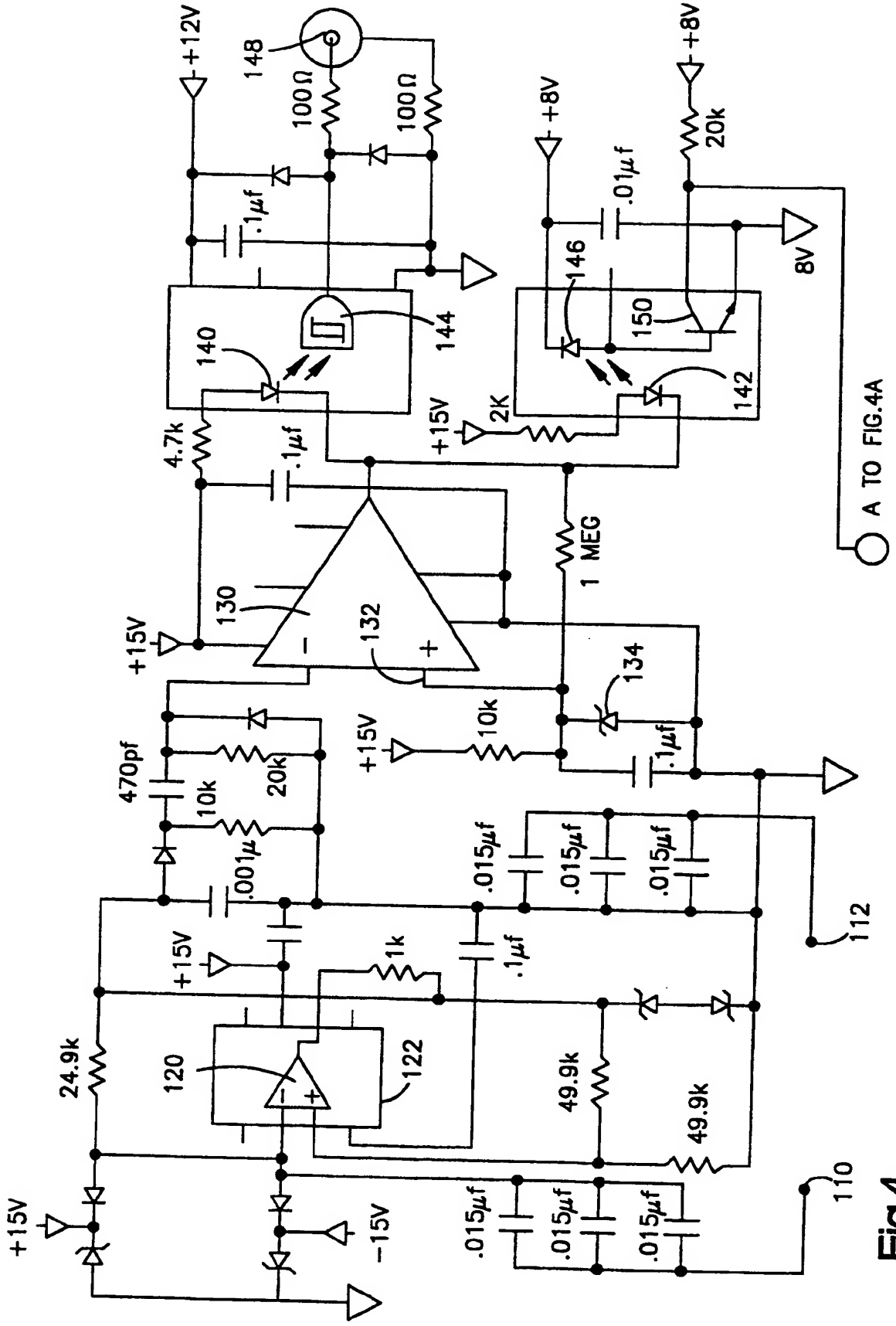

Fig.4

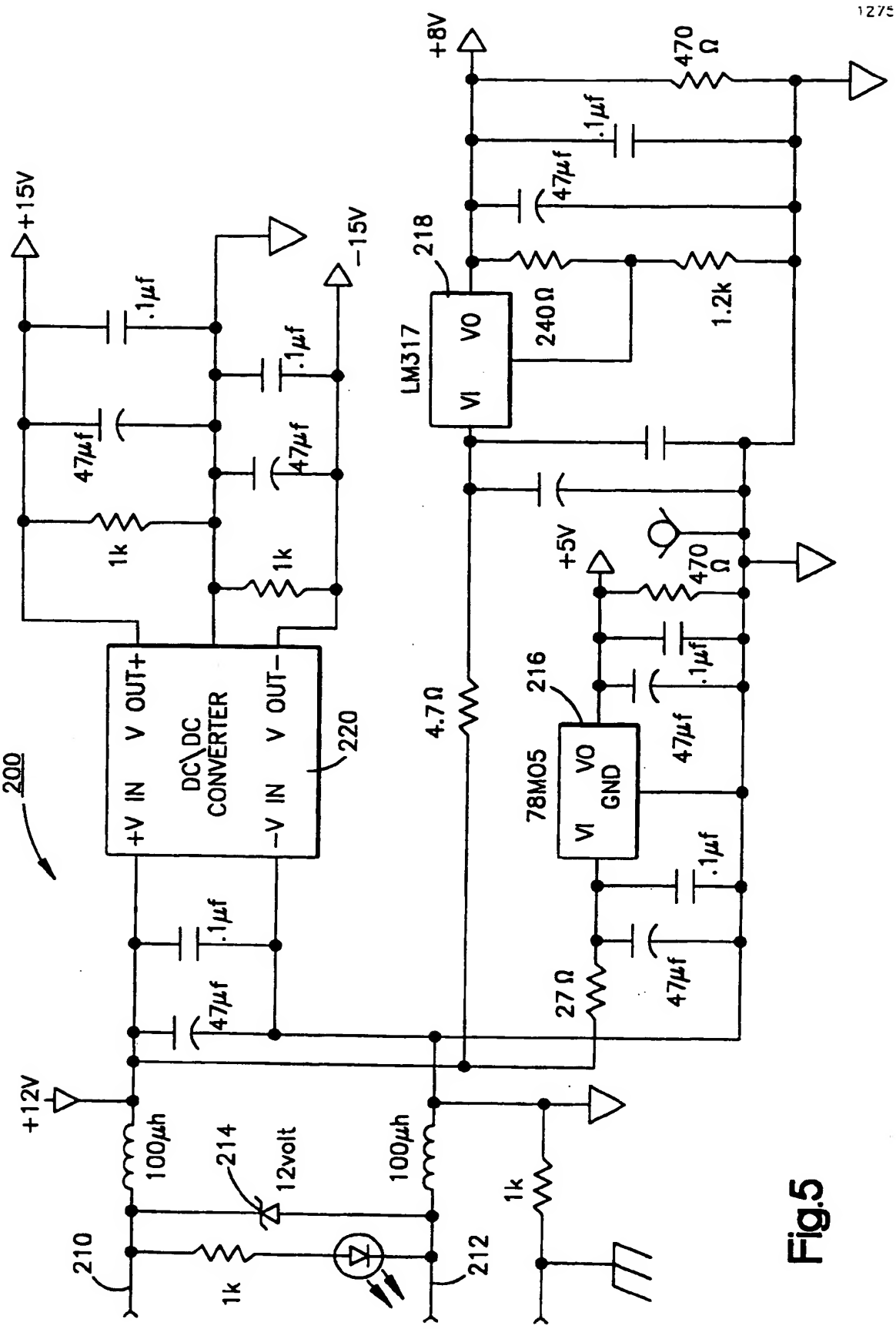

Fig.5

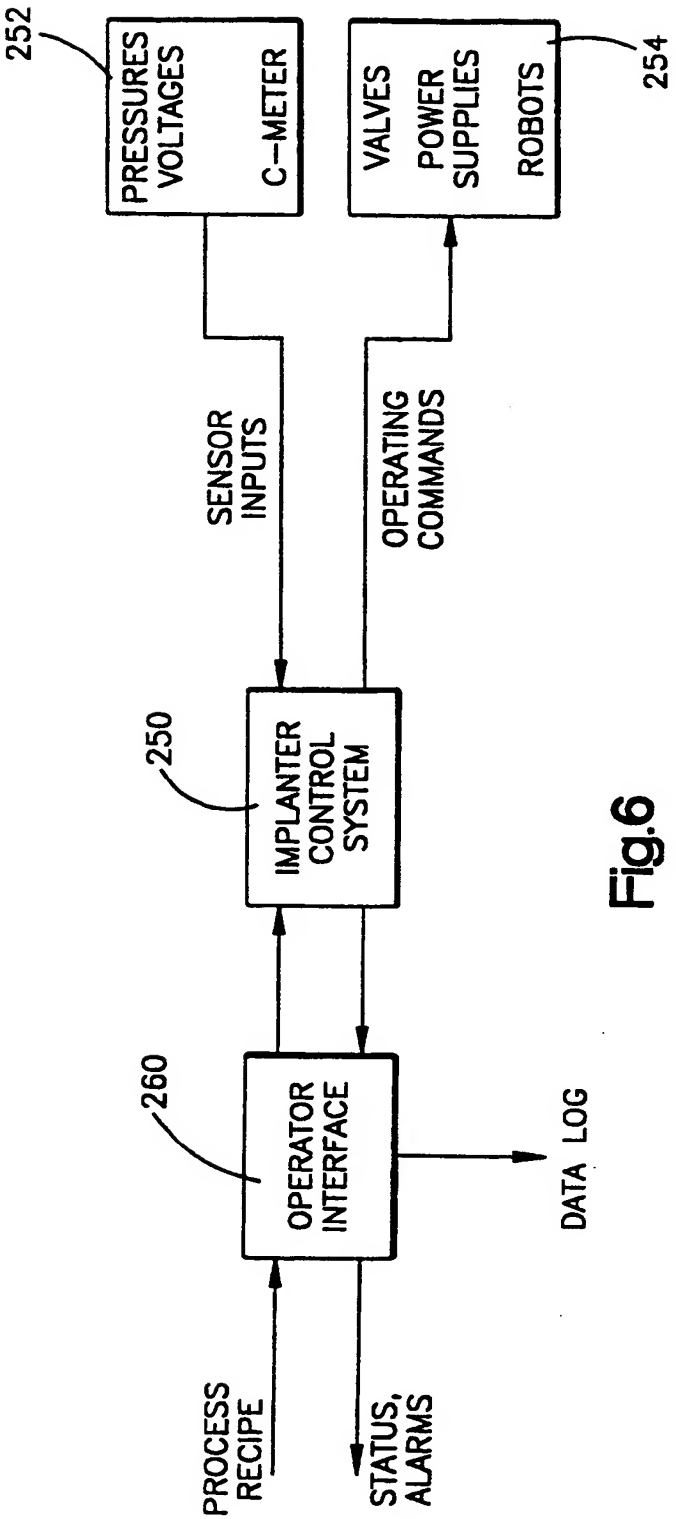

Fig.6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 30 0237

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
Y	FR-A-2 676 603 (HORWITZ) * page 14, line 13 - page 22, line 22; figures 1-7 *	1-5,7	H01L21/00
D,Y	US-A-5 103 367 (HORWITZ) * the whole document *	1-5,7	
A	US-A-4 733 632 (OHMI) * figures 9A,9B *	6	
D,A	US-A-4 261 762 (KING)		

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L
C23C

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	30 March 1994	Bertin, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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